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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,657	12/18/2001	Gilbert Wolrich	10559/613001/P12852	2667

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EXAMINER	
PATEL, JAY P	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/024,657	WOLRICH ET AL.	
	Examiner	Art Unit	
	Jay P. Patel	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-19,21-31 and 33* is/are rejected.

7)☒ Claim(s) *14, 20, 32 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment/remarks filed 10/26/2006.

2. This office action has been made final.

3. Claims 1-34 are pending.

4. Claims 1-13, 15-19 and 21-31 and 33 are rejected.

5. Claims 14, 20, 32 and 34 are objected to.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 9-13, 15-19, 21-25, 29-31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr (US Patent 6470415 B1) in view of Westbrook et al. (US Patent 7092393 B1).

8. In regards to claim 1, Starr teaches in figure 1 an enqueue operation 60 (written to head units 33 or 35) and a dequeue operation 62 (read from tail units 37 or 39). The enqueue operation 60 and dequeue operation 62 read on a first enqueue request and a second dequeue request respectively. Figure 3 is the network computer apparatus where the management of the queues of figure 1 takes place. Figure 5 is the detailed diagram of the queue manger 220 disclosed in figure 3. Starr reveals that the operation of the queue manager is pipelined (column 5, lines 4-5) and discloses an SRAM

controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 reads on causing to commence processing of the second request prior to completion of processing the first request.

Starr fails to teach, causing to store information describing a structure of the queue in a cache memory implemented in a distributed manner. Westbrook teaches the above-mentioned limitation. Westbrook shows in figure 4A, resequencer and reassembly components 303 A, C-D, received over ring 304 B. Figure 5 is a detailed diagram of packet resequencer 402 from figure 4A and contains data structure cache RAM 514. Global and local data structures are updated and stored in RAM 514 (see column 12, lines 64-66).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement a cached memory distribution structure as disclosed by Westbrook in the eneque-dequeue operation disclosed by Starr. The motivation to do so would be to have more dynamic allocation to store queue structure information.

In regards to claim 2, Starr teaches that QRAM 245 in figure 5, stores pointers regarding each queue (see column 5, lines 12-18). The arbiter 235 selects an operation and modifies the variables of QRAM 245 (see column 5, lines 19-23). The pointers anticipate modifying stored information describing a structure of the queue in response to the requests.

In regards to claim 3, the pointers are stored in a QRAM 245. Therefore, the QRAM anticipates storing the modified information in a cache memory.

In regards to claim 4, The QRAM 245 stores pointer relating to the queue as variables related to the queues (see column 5, lines 12-18). Therefore, the QRAM reads on the first and second requests using linked list data structure.

In regards to claim 5, the enqueue operation 60 and dequeue operation 62 anticipate a first enqueue request and a second dequeue request respectively.

9. In regards to claim 9, figure 2 includes a queue controller 14, which handles enqueuing and dequeuing of entries. Therefore, the queue controller 14 anticipates a processing engine to make enqueue requests and a scheduler to make dequeue request.

Figure 5 includes a QRAM 245 that stores pointers regarding each queue (see column 5, lines 12-18). Therefore, the QRAM 245 anticipates a cache memory to store data describing a structure of a queue

Figure 5 is an illustration of a queue manager 220. The queue manager 220 anticipates a queue manager including a content addressable memory to store a reference (pointer stored in QRAM 245) to data in the cache memory (QRAM 245) describing the structure of the queue.

Starr also reveals an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 anticipates the queue manager configured to process the enqueue requests and the dequeue requests and capable of commencing processing a request to a queue while a previous request with respect to same queue is being processed.

In further regards to claim 9, Starr fails to teach a memory controller to initiate queue commands and distributing the cache memory partially to the memory controller. Westbrook teaches the above-mentioned limitations. Westbrook shows in figure 4A, resequencer and reassembly components 303 A, C-D, received over ring 304 B. Figure 5 is a detailed diagram of packet resequencer 402 from figure 4A and contains data structure cache RAM 514. Global and local data structures are updated and stored in RAM 514 (see column 12, lines 64-66). Memory controller 516 controls RAM 520, which stores additional resequencing local and global data structures (see column 13, lines 5-8).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement a cached memory distribution structure as disclosed by Westbrook in the eneque-dequeue operation disclosed by Starr. The motivation to do so would be to have more dynamic allocation to store queue structure information.

In regards to claim 10, DRAM 203 and SRAM 206 anticipate memory to store data placed on a queue.

In regards to claim 11, Starr teaches that the operation in the queue manager is pipelined (see column 5, lines 4-5). Therefore, the pipelined queue manger operation anticipates a plurality of multi-threaded pipelined programming engines, configured in a pipeline to receive, assemble, and classify data packets to determine an output queue for each packet and to make requests to the queue manager that specify the output queue.

In regards to claim 12, the SRAM controller 214 in figure 3 is coupled to transmit sequencer 215 and queue manager 220. Therefore, the second plurality of pipelined programming engines to receive data from the queue manager and send data to a transmit buffer is anticipated by the connection between the transmit sequencer, the queue manger and the SRAM controller 214.

In regards to claim 13, the transmit sequencer 215 anticipates a scheduler configured to determine the order of packets to be removed from the queue. Figure 4 contains four registers; a positive setting for a specific bit in the Q-Empty register 86 indicates an empty queue (column 4, lines 43-44). The Q-Empty register anticipates a bit for the queue indicating whether the queue is empty.

10. In regards to claim 15, host 170 in figure 3 anticipates a source of data packets.

Device 160 in figure 3 is connected to a network 164. Therefore it is inherent that there is a destination for the data packets.

In further regards, figure 2 includes a queue controller 14, which handles enqueuing and dequeuing of entries. Therefore, the queue controller 14 anticipates a processing engine to make enqueue requests and a scheduler to make dequeue request.

Figure 5 includes a QRAM 245 that stores pointers regarding each queue (see column 5, lines 12-18). Therefore, the QRAM 245 anticipates a cache memory to store data describing a structure of a queue

Figure 5 is an illustration of a queue manager 220. The queue manager 220 anticipates a queue manager including a content addressable memory to store a reference (pointer stored in QRAM 245) to data in the cache memory (QRAM 245) describing the structure of the queue.

Starr also reveals an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 anticipates the queue manager configured to process the enqueue requests and the dequeue requests and capable of commencing processing a request to a queue while a previous request with respect to same queue is being processed.

In further regards to claim 15, Starr fails to teach a memory controller to initiate queue commands and distributing the cache memory partially to the memory controller. Westbrook teaches the above-mentioned limitations. Westbrook shows in figure 4A, resequencer and reassembly components 303 A, C-D, received over ring 304 B. Figure 5 is a detailed diagram of packet resequencer 402 from figure 4A and contains data structure cache RAM 514. Global and local data structures are updated and stored in RAM 514 (see column 12, lines 64-66). Memory controller 516 controls RAM 520, which stores additional resequencing local and global data structures (see column 13, lines 5-8).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement a cached memory distribution structure as disclosed

by Westbrook in the eneque-dequeue operation disclosed by Starr. The motivation to do so would be to have more dynamic allocation to store queue structure information.

11. In regards to claim 21, Starr reveals that the operation of the queue manager is pipelined (column 5, lines 4-5) and in particular, an SRAM controller 214 in figure 3 which services the read and write requests by reading the tail or writing the head of the accessed queue (see figure 3 and column 5, lines 36-40). The SRAM controller 214 and the pipelined process of the queue manager anticipates causing to commence processing of a received enqueue or dequeue request with respect to a queue prior to completion of processing a prior enqueue or dequeue request with respect to the same queue.

Starr fails to teach, causing to store information describing a structure of the queue in a cache memory implemented in a distributed manner. Westbrook teaches the above-mentioned limitation. Westbrook shows in figure 4A, resequencer and reassembly components 303 A, C-D, received over ring 304 B. Figure 5 is a detailed diagram of packet resequencer 402 from figure 4A and contains data structure cache RAM 514. Global and local data structures are updated and stored in RAM 514 (see column 12, lines 64-66).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement a cached memory distribution structure as disclosed by Westbrook in the eneque-dequeue operation disclosed by Starr. The motivation to do so would be to have more dynamic allocation to store queue structure information.

In regards to claim 22, Starr teaches that QRAM 245 in figure 5, stores pointers regarding each queue (see column 5, lines 12-18). The arbiter 235 selects an operation and modifies the variables of QRAM 245 (see column 5, lines 19-23). The pointers anticipate modifying stored information describing a structure of the queue in response to the requests.

In regards to claim 23, the pointers are stored in a QRAM 245. Therefore, the QRAM anticipates storing the modified information in a cache memory.

In regards to claim 24, The QRAM 245 stores pointer relating to the queue as variables related to the queues (see column 5, lines 12-18). Therefore, the QRAM reads on the first and second requests using linked list data structure.

In regards to claim 25, the enqueue operation 60 and dequeue operation 62 anticipate a first enqueue request and a second dequeue request respectively and commencing the processing of the second (dequeue operation 62) prior to the completion of the first request (enqueue operation 60).

In regards to claims 29 and 30, Starr in combination with Westbrook teaches all the limitations of parent claim 1 as stated above. Starr fails to teach however, the cache memory distributed to the queue manager and a memory controller. Westbrook teaches the above-mentioned limitation. Figure 5 contains memory controller 516 and figure 4A has queue manager 415 within the distributed reassembly and resequencer components of figure 3. Furthermore, all the components reside outside of processor 102 in figure 1A.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement a cached memory distribution structure as disclosed by Westbrook in the eneque-dequeue operation disclosed by Starr. The motivation to do so would be to have more dynamic allocation to store queue structure information.

In regards to claims 31 and 33, Starr in combination with Westbrook, teaches all the limitations of parent claims 9 and 15. Starr however fails to teach cache memory partially distributed to the queue manager.

Figure 4A has queue manager 415 within the distributed reassembly and resequencer components of figure 3.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to implement a cached memory distribution structure as disclosed by Westbrook in the eneque-dequeue operation disclosed by Starr. The motivation to do so would be to have more dynamic allocation to store queue structure information.

12. Claims 6-8 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Starr (US Patent 6470415 B1).

13. In regards to claims 6-8 and 26-28, Starr teaches all the limitations of the parent claims 1 and 21 as stated above. Starr fails to explicitly show the first request being dequeue request and the second request being an enqueue request or the first and second request both being enqueue requests and the first and the second requests being dequeue requests.

However, it would have been obvious to one skilled in the art at the time the invention was made to modify the operations of the SRAMs 22 and 30 and DRAM 25 in

figure 1 to enable the queue manager 220 (figure 3) to perform the first and second operations as dequeue/enqueue, enqueue/enqueue and dequeue/dequeue requests. The advantage of doing so would enable the queue manager to dynamically perform memory read/write operations in any given order in order to better manage the flow of data through a network apparatus. For example some data may be enqueued in both the SRAM and the DRAM or may to be dequeued and enqueued from one memory to another or may be dequeued from both memories. The motivation to modify would be to have a queue manager that performs all the necessary memory read/write operations in any order possible for better memory control.

Conclusion

Claims 14, 20, 32 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay P. Patel whose telephone number is (571) 272-3086. The examiner can normally be reached on M-F 9:00 am - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPP 12/16/06
Jay P. Patel
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